Integrated Device Technology, Inc.

2M x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4084

FEATURES:

- High-density 16 megabit (2M x 8) Static RAM module
- Equivalent to the JEDEC standard for future monolithic
- Fast access time: 55ns (max.)
- Low power consumption
  - — Active: 110mA (max.)
  - — CMOS Standby: 450µA (max.)
  - — Data Retention: 250µA (max.) Vcc = 2V
- Surface mounted plastic packages on a 36-pin, 600 mil FR-4 DIP (Dual-In-Line Package) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible

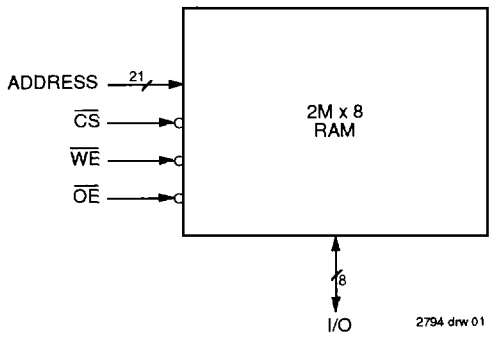
DESCRIPTION:

The IDT7M4084 is a 16 megabit (2M x 8) Static RAM module constructed on a co-fired ceramic substrate using four 512K x 8 Static RAMs and a decoder. The IDT7M4084 is available with access times as fast as 55ns, and a data retention current of 250µA and a standby current of 450µA.

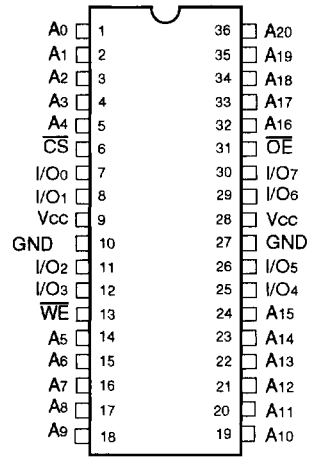
The IDT7M4084 is packaged in a 36-pin ceramic DIP resulting in the same JEDEC footprint in a package 1.9 inches long and 0.6 inches wide.

All inputs and outputs of the7M4084 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP
TOP VIEW

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-20	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

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CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

NOTE:
1. This parameter is guaranteed by design, but not tested.

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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

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1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:

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1. V_{IL} = -2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

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DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	7M4084LxxN		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	20	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$; f = f_{MAX}, Outputs Open	—	110	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	12	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V	—	450	µA

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DATA RETENTION CHARACTERISTICS

(T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max. V_{CC} @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	250	µA
t_{CDR}(2)	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V or	0	—	ns
t_R(2)	Operation Recovery Time	$V_{IN} \geq 0.2V$	t_{RC}(1)	—	ns

NOTES:
1. t_{RC} = Read Cycle Time.
2. This parameter is guaranteed by design, but not tested.

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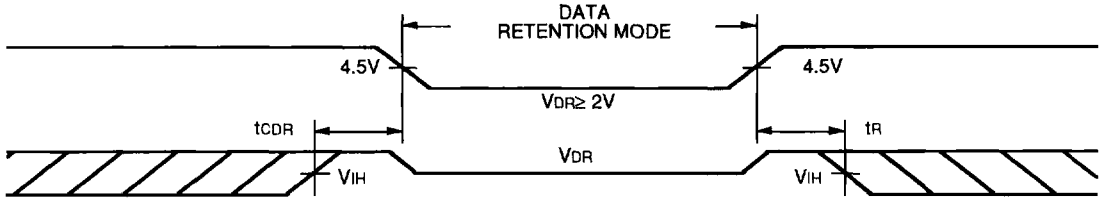
DATA RETENTION WAVEFORM



2794 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2794 tbl 09

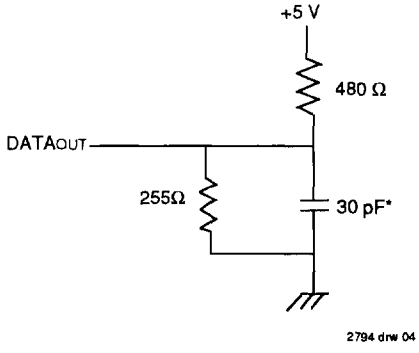


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Figure 1. Output Load

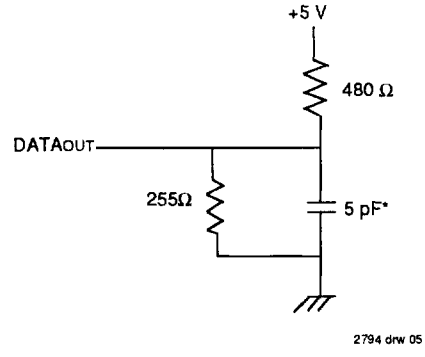

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Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

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AC ELECTRICAL CHARACTERISTICS[2]

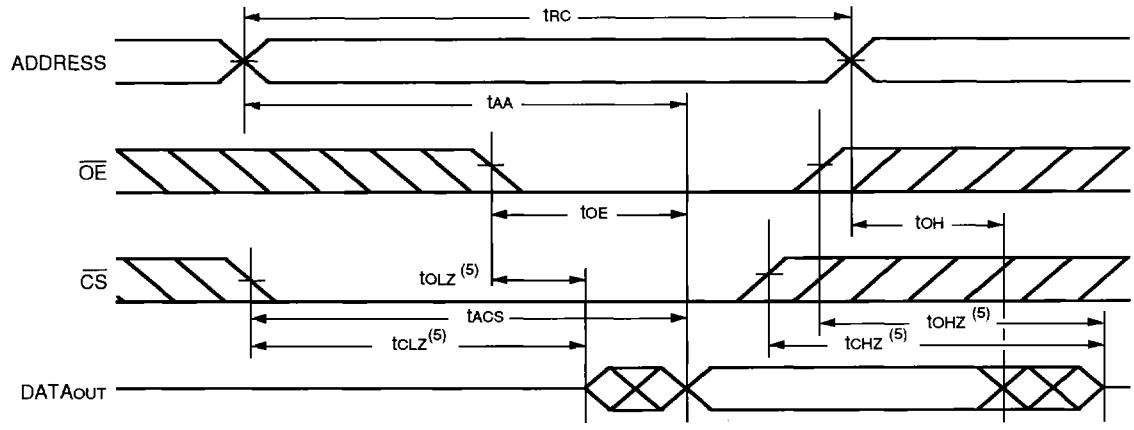
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7M4084LxxN										Unit
		-55		-70		-85		-100		-120		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	55	—	70	—	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	55	—	70	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	30	—	45	—	48	—	50	—	60	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	—	20	—	30	—	33	—	35	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	5	—	5	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High-Z	—	20	—	40	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	55	—	70	—	85	—	100	—	120	ns
Write Cycle												
t_{WC}	Write Cycle Time	55	—	70	—	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	55	—	55	—	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	5	—	0	—	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End-of-Write	50	—	65	—	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End-of-Write	50	—	65	—	80	—	85	—	100	—	ns
t_{DW}	Data to Write Time Overlap	20	—	35	—	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	—	20	—	30	—	33	—	35	—	40	ns
t_{OW}[1]	Output Active from End-of-Write	5	—	0	—	0	—	0	—	0	—	ns

NOTES:
2794 tbl 10

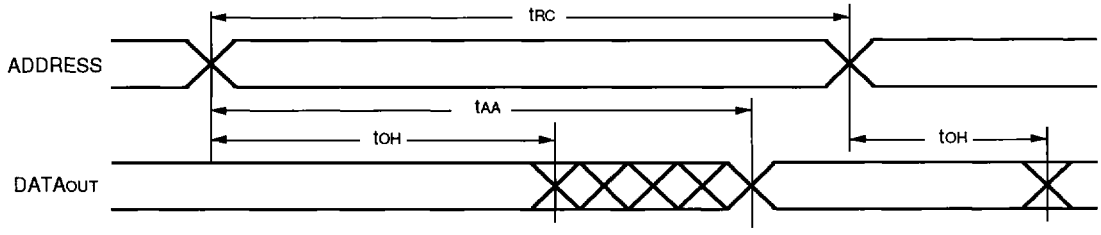
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



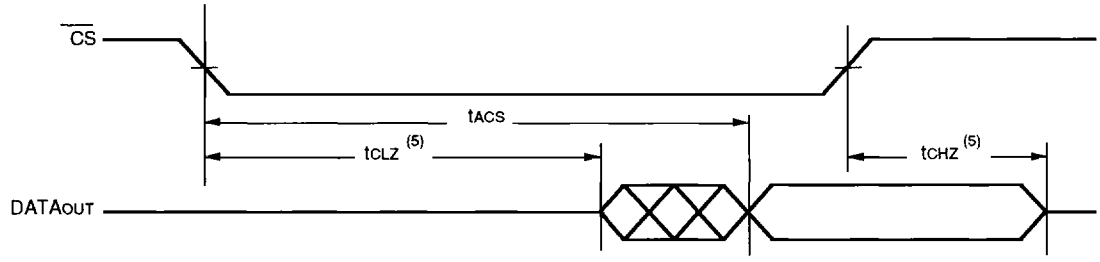
2794 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



2794 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



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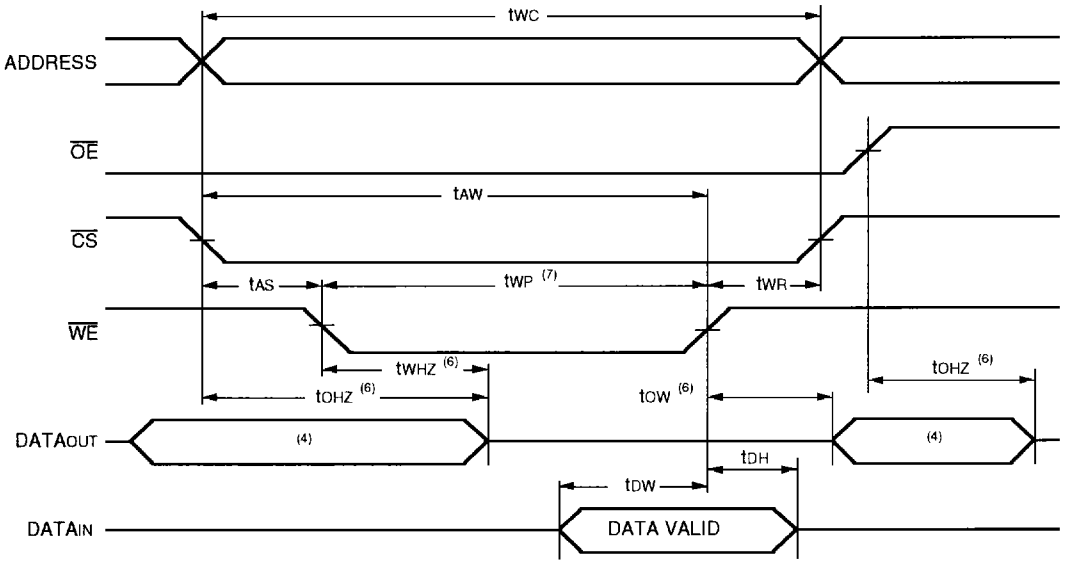
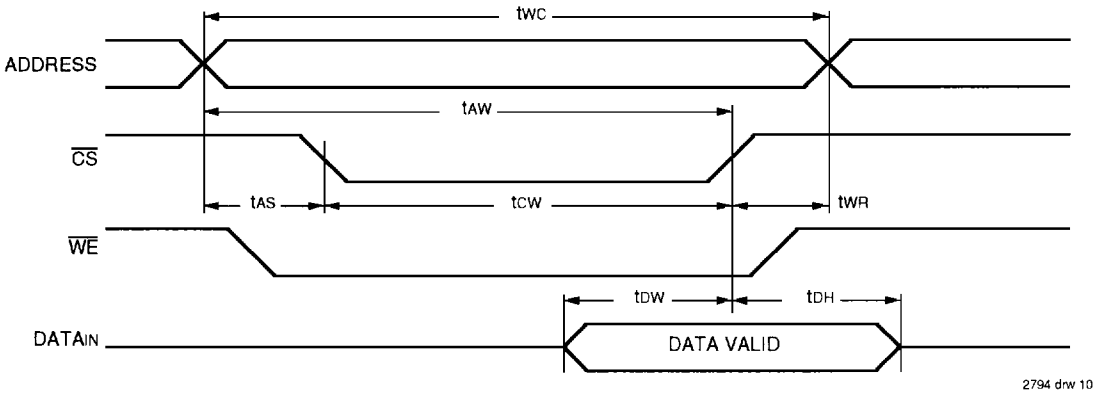
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



2794 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



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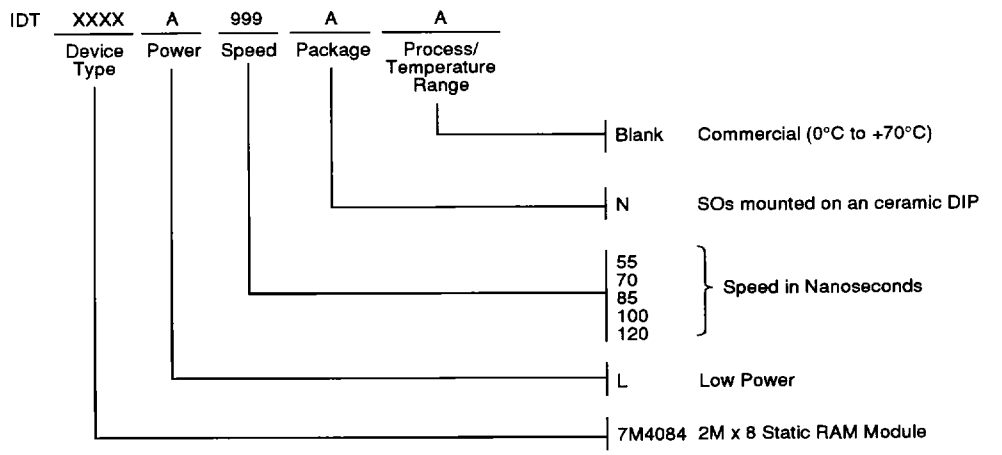
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater of tWP or tWHZ + tDW to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS

TBD

(Please Consult Factory)

ORDERING INFORMATION



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